Disruptive Developments for Advanced Die Attach to Tackle the Challenges of Heterogeneous Integration

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ABSTRACT

In spite of the fact that Moore's law ("more Moore") is slowing down the targets of the electronics industry to reduce cost and power of electronic functions by a factor of 10.000 over the next 15 years will not be given up. Heterogeneous integration ("more than Moore") is the approach which is believed to support the progress when Moore's law cannot help any more.

Die attach, which was not a crucial packaging step in the past seems in future to carry a major role as 'Advanced Die Attach', where cost pressure drives to both faster pick and place cycles and larger working area, while novel interconnect processes like hybrid bonding require extremal clean capabilities, which are currently only observed in front-end environments, at the same time asking for ultra accurate placements in the nanometer scale for 2.5D and 3D integration challenges in combination with enhanced small die and thin die capability.

To meet these roadmap goals the development of die attach equipment has to pass disruptive revolution steps, which is the objective of this contribution.

Keywords—die attach; advanced packaging; 3D-SIC; 3D-SOC, fan-out packaging; thermo-compression bonding, panel level packaging, hybrid bonding, transfer printing

1. INTRODUCTION

No industry branch can exhibit as much progress and innovation as the semiconductor and electronics industry, which has been driven over a half century by the pace making of Moore's law [1], originally a prediction of Gordon Moore that transistor density in an integrated circuit will double every year. But beyond the nature of a pure prediction Moore's law (in slightly adapted form) became a joint industry commitment to scale transistor density according to Moore's prediction, a "free riding ticket" to guarantee technology improvement for an endless series of new consumer products by decreasing cost per function, thus an approach bringing sufficient payback for the required R&D investments to continue Moore's law.

But advanced transistor scaling is reaching its physical limits, and it is more and more difficult and costly to reduce the feature size [2]. A growing community of believers, who work as volunteers on the Heterogeneous Integration Roadmap (HIR), is postulating that both cost and power consumption per electronic function can be decreased by a factor of 10.000 in the next 15 years by applying the approach of heterogeneous integration [3], building complex systems comprising passives and active dissimilar die, being integrated into a system by utilizing advanced packaging technologies ("More than Moore"), rather than integrating most of the functions into a single chip and going for finer feature sizes.

With the paradigm of heterogeneous integration (HI) the semiconductor packaging, originally considered as a pure protection of the bare semiconductor die, carries now one of the key roles to progress along the roadmap targets of the heterogeneous integration roadmap. In this sense it should be obvious that a lot of disruptive developments will be seen in the near future regarding packaging technology. In this paper the focus is on disruptive approaches in advanced die attach technology, a small, but in future crucial subset of heterogeneous integration technology.

2. STATE-OF-THE-ART INTEGRATION ARCHITECTURES

In a heterogeneous integrated system dissimilar chips with different functions from different foundries, wafers and feature sizes are integrated into a system or subsystem. How should these dissimilar chips talk to each other?

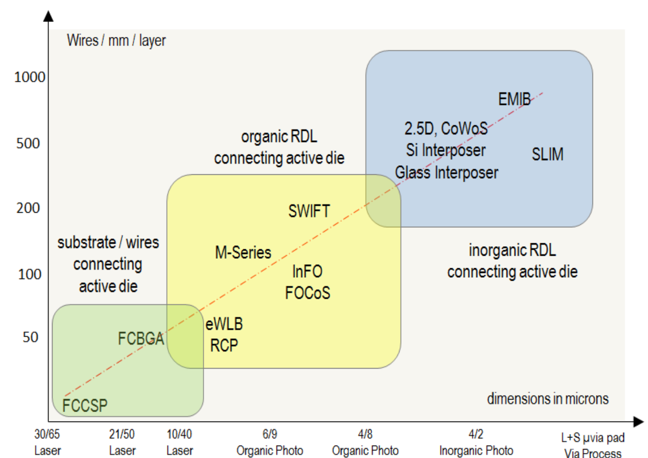

Figure 1: Multi-chip package architecture comparison with respect to linear density (based on: Raja Swaminathan / Intel [4])

To answer this question it is helpful to draw a landscape of

2D/2.5D/3D integration architectures with respect to linear interconnect density. Figure 1 is an outcome of such approach, which has been originated by experts of the heterogeneous integration roadmap and has been presented as some intermediate summary in [4].

The approach separates architectures into three categories. On the low-end side there is the family of conventional 2D multi-chip package (MCP) architectures, including e.g. FCCSPs and FCBGAs, where interconnection of active side-by-side die is accomplished by either (wire bonded) wires and/or substrate wire traces. Typical wire density is up to 50-60 per mm per layer [4], but substrate manufacturers are working hard to push the boundary into the region of 250 wires per mm per layer (2µ/2µ line spacing) [5].

On the mid-end side a lot of new technologies have been developed based on organic RDL based fan-out wafer/panel level packaging. The typical line spacing is 10µ/10µ downto 5µ/5µ which supports typical wire densities of 50 to 100 wires per mm per layer, and there is development to reach the 2µ/2µ area. Cost effective fan-out packaging technologies with coarse line spacing are eWLB [6], RCP [7] and M-Series [8], while InFO [9] and SWIFT [10] enable finer line spacing. There are also approaches like FOCoS where active die are first connected side by side as a fan-out package, which is afterwards assembled onto a substrate [4].

On the high-end side there are 2.5D, 2.5D-like and 3D technologies, where interconnection between active die is either done directly (3D) or by an inorganic RDL (2.5D, 2.5D-like). The classical 2.5D architecture comprises a passive silicon interposer with through-silicon-vias (TSVs) on which active die are assembled and connected side-by-side with an inorganic (silicon oxide or silicon nitride) RDL [11]. Similar to silicon interposers are glass interposers [12]. An alternative cost effective architecture, which also overcomes the size constraints of interposers due to the limitation of reticle sizes, is the Embedded Multi-Die Interconnect Bridge (EMIB) architecture, which also utilizes inorganic high density RDL [13]. Finally the SLIM architecture is a hybrid construct of frontend-processed inorganic high density RDL and middle-end processed organic RDL [14]. Similar to FOCoS a 2.5D interposer package can be assembled onto a substrate to improve board level reliability, which e.g. is the case for the CoWoS architecture [15]. All 2.5D and 2.5D-like architectures support line spacing downto the sub-micron range, achieving a linear wire density of 1000 wires per mm per layer.

The same linear density can be achieved for 3D structures where connection between active die is direct (without agency of the package), either by stacking of TSV-die or by TSV-less face-to-face assembly.

3. Next Generation Integration Architectures

For TSV-based 3D architectures IMEC's 3D integration roadmap [16] gives further indication about a pitch roadmap for 3D integrated architectures (figure 2). The roadmap distinguishes between 3D stacked ICs (3D-SIC) with a pitch roadmap from 40 µm down to 5 µm at global level, and between 3D-System-on-Chip devices (3D-SOCs), with a pitch roadmap from 5 µm down to 1 µm at the semi-global level. 3D-SICs are now very popular devices in 3D-memory application area, known as hybrid memory cube (HMC), high bandwidth memory (HBM) and stacked DDR, all being assembled using thermo-compression bonding, which seems to be a viable bonding method for the 20µ and greater pitch spectrum. For pitches of 10µ and below thermo-compression bonding gets seriously difficult [17].

For this reason efforts have been put into the development of the hybrid bonding process which is seen by experts as the feasible method to build 3D-SICs and 3D-SOCs with pitches of 10µ and below. In [18] the future landscape of 2.5D and 3D is sketched with a summarizing claim that submicron pitch can be envisioned for hybrid bonding.

	3D-SIC	3D-SOC		
wiring level	Global	Semi-global	Intermediate	Local
2-tier stack				2nd FEOL after stacking
Contact Pitch *Relative density:*	40 ⇒20 ⇒10 ⇒5µm 1/16⇒1/4 ⇒1 ⇒4	5 ⇒ 1 µm 4 ⇒ 100	2 µm ⇒ 0.5 µm 50 ⇒ 400	200 ⇒ 100 nm 5000 ⇒ 10000
Partitioning	Die	**blocks** of standard cells		**Gates**

Figure 2: IMEC's 3D integration roadmap

3D-SOCs based on wafer-to-wafer (W2W) hybrid bonding are already in mass production for CMOS image sensors with 6µm pitch [19,20], and the industry is working now on the chip-to-wafer (C2W) version of hybrid bonding [20], which for pitches of 1-5µ would open the door to an area interconnection density of 40.000 to 1 million bumps per mm^2 and beyond.

Interconnection at such large areal density level is seriously studied for disintegration of 2D-SOCs into heterogeneously integrated 3D-SOCs, comprising processing (logic), memory (SRAM) and I/O layer [16].

Besides of the 3D focus such large areal density is considered as an enabler for new 2.5D heterogeneous integration platforms, based on so called dielets or chiplets. In [21] a chiplet is defined as a functional, verified, re-usable IP block, realized in physical form.

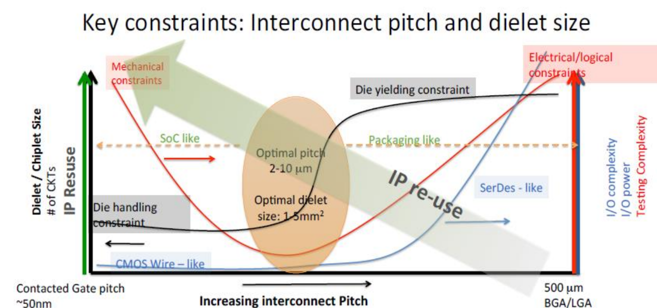

Figure 3: Pitch sweet spot between 2 and 10µm for dielet/chiplet based HI platforms (source: S. Iyer / UCLA [23])

DARPA is running the CHIPS program in collaboration with industrial and academic partners, which addresses such 2.5D based heterogeneous chiplet integration, targeting 10 Gpbs data rate, <1pJ/bit energy efficiency, <5ns latency and >1000 Gbps band width density [22], a program developing design tools, integration standards and IP blocks required to demonstrate modular electronic systems that can leverage the best of military and commercial designs and technology.

In [23] a study about pitch requirements for a chiplet/dielet platform like CHIPS has been published, which identifies a sweet spot for inorganic RDL based interconnect pitches between 2-10 µm leveraging an optimum compromise between mechanical and electrical/logical as well as die handling and die yielding constraints (figure 3). Such pitch range translates to areal density of 10.000 to 250.000 bumps / mm^2.

4. High Placement accuracy Drivers

An important metrics for heterogeneous integration architectures is bump pitch, which is also a measure of areal interconnect density. Both quantities can be converted into each other by the relation

$$\text{areal density} = 1 / (\text{bump pitch})^2.$$

Figure 4 clusters and visualizes the discussed HI architectures in a double logarithmic plot where areal density (left vertical scale) as a function of bump pitch (horizontal scale) appears as a straight line. The right vertical scale shows the associated placement accuracy, where the rule of thumb

$$\text{placement accuracy @ } 3\sigma = (\text{bump pitch}) / 10$$

has been applied for placement accuracy, which for self centering processes (like mass reflow flip chip) has to be interpreted as die center placement accuracy, otherwise to be considered as the placement accuracy for each bump location, which is additionally influenced by rotational accuracy.

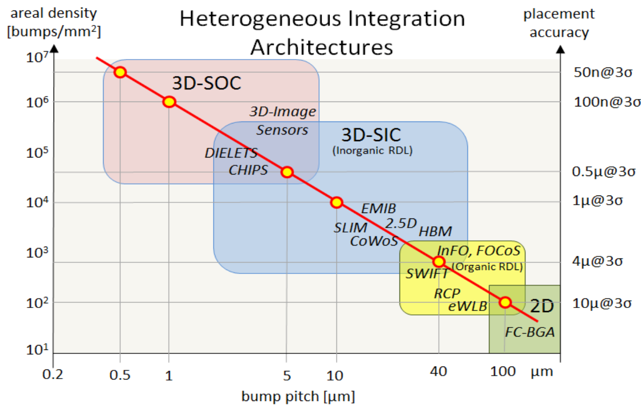

Figure 4: Comparison of Heterogeneous Integration architectures according to bump pitch metrics and areal density.

From the study of previous section and the summary of figure 4 it can be concluded that a placement accuracy is demanded of 1µ@3σ down to 200nm@3σ for dielet/chiplet platforms at each corner, which for C2W based 3D-SOCs drives down to 50nm@3σ.

It should be realized that such high placement accuracy in combination with a productive placement process can only be solved with a hybrid bonding approach [17,18,20]. This means, in addition to the high placement accuracy an advanced die attach equipment has also to provide an extreme clean environment, which is considered to be ISO-3 clean class (clean class 1).

5. Cost Reduction Drivers

While high placement accuracy is the requirement for the achievement of high interconnect density there are many applications, especially coming from mobile and IoT area, without the need of higher interconnect density, but with extreme pressure on package cost reduction. Wafer and panel level fan-out packaging (WL-FO/PL-FO) is expected to be a proper answer to such cost reduction pressure, and it is expected that PL-FO packages will beat flip-chip packages in terms of cost while maintaining the reliability properties. There are studies which claim that PL-FO packages can be made cheaper than wire-bonded lead frame packages for some die and package size combinations. Figure 5, e.g., shows that PL-FO packages up to 400 I/O with package size < 8 x 8mm can be made cheaper than a corresponding wire-bonded lead frame package [24,25].

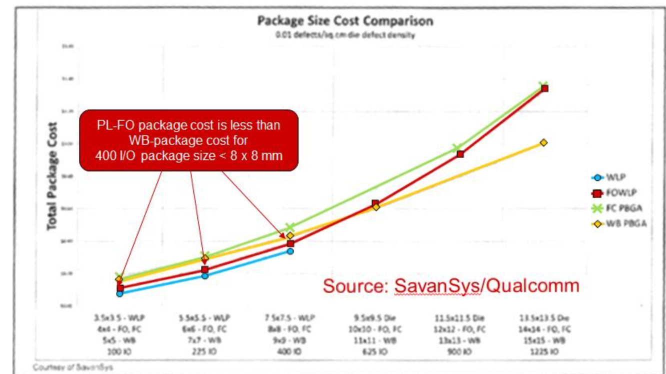

Figure 5: Package size cost comparison: PL-FO package cost is less than WB-package cost for 400 I/O package size < 8 x 8mm.

The costs of fan-out packages are majorly determined by RDL costs and pick and place costs. While pick and place costs are more or less not influenced by the panel size of the PL-FO process, the RDL costs are primarily batch related [26], thus are reducing in inverse proportion with the panel size.

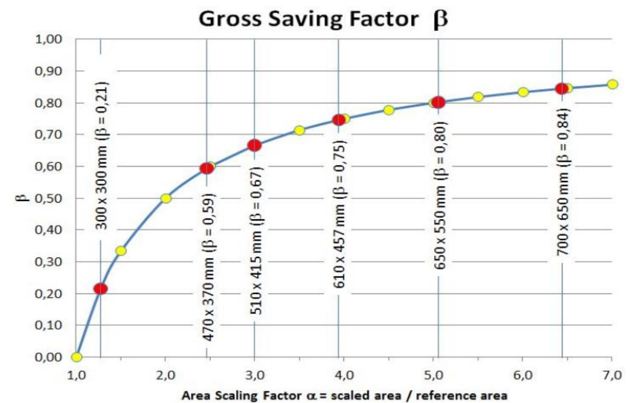

Figure 6: Gross saving factor β as a function of area scaling factor α for circular ϕ300mm reference area. $\beta = 1\text{-}1/\alpha$ tells the savings due to α-scaling if γ=100% of the costs would be batch related. For e.g. γ=35% batch related costs the total savings are $\gamma{\cdot}\beta = 35\%{\cdot}\beta$

Figure 6 shows graphically the dependence of the gross saving factor β (percentual gross savings, if all costs would be

batch-related) as a function of area scaling α (ratio of scaled area divided by a reference area, e.g. 300 mm carrier area). A take-away from figure 6 is that by moving from circular 300 mm area to a GEN-3 panel size (650x550mm) the gross savings are about 80%, which means that such scaling step utilizes already the 80%-majority of gross savings [26].

Besides the reduction of RDL costs, which are primarily batch related costs, and which are scaling down with growing panel size, the pick and place costs have to be reduced. Here it is expected that the throughput of die attach machines has to be increased by at least a factor of 3 to 4. There are new disruptive approaches based on a mass transfer of micro-scale devices, which is called transfer printing in some context. Such kind of pick and place approach does not peel die from a dicing frame, instead die are stamped out from a special processed wafer which supports transfer-print compatible micro devices that are undercut and anchored using MEMS-processing technologies (figure 7) [27]. In contrast to low cost panel level packaging such process demands considerable high accuracy, such as 1.5µ@3σ [27].

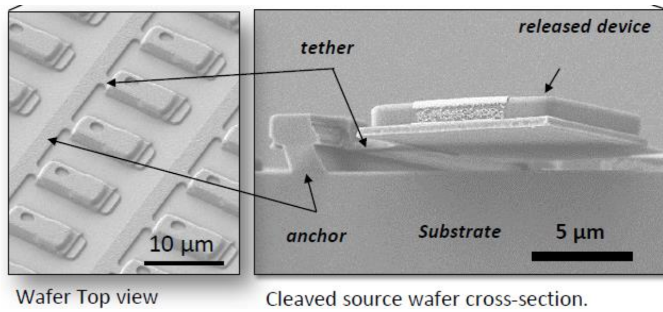

Figure 7: Example of transfer-print compatible micro devices (source: K. Ghosal / X-Celeprint [27])

6. Disruptive Demand For Higher Capabilities

Based on the assessment in previous sections it may be concluded that 4 main capabilities are required for Advanced Die Attach equipment:

1) Enhanced accuracy of 500nm@3σ at 300 mm wafer level with a roadmap down to 50 nm@3σ for hybrid bonding processes.
2) High accuracy of 1.5µ@3σ for interposer bridge embedding (EMIB like) and transfer printing on large panel level, with a roadmap down to 500nm@3σ.
3) Enhanced clean capability ISO-4 with a roadmap down to ISO-2 for hybrid bonding processes [20,28].
4) Enhanced working area for GEN-3 panels (650 x 550 mm) and a roadmap to at least GEN-4.5 (920 x 730 mm)
5) Enhanced throughput with 15.000 components per hour (CPH) with a roadmap to 40.000 components per hour, picked from a single wafer.

Since all these requirements are driven by specific applications it is worth to study a summary telling which applications are exactly driving which requirements (table 1).

Application	Accuracy	Clean Class	Throughput	Working Area
2D-FCBGA (mass reflow)	5-10µ@3σ (die center)	ISO-6	15-20 kCPH	300 x 125 mm
WL/PL-FO (organic RDL)	3-10µ@3σ (die corners)	ISO-5	15-40 kCPH	ϕ 300 mm 650 x 550 mm
WL-FO (inorganic RDL)	2-3µ@3σ (die corners)	ISO-5	5-10 kCPH	ϕ 300 mm
3D-SICs (TC bonding)	2-3µ@3σ (die corners)	ISO-5	3-5 kCPH (tack & gang)	ϕ 300 mm
Classical 2.5D (mass reflow)	3-5µ@3σ (die center)	ISO-5	5-10 kCPH	ϕ 300 mm
Bridge Embedding	0.5-2µ@3σ (die corners)	ISO-4	2-5 kCPH	650 x 550 mm
Dielet Platform (hybrid bonding)	0.2-1µ@3σ (die corners)	ISO-3 (ISO-2)	5-10 kCPH	ϕ 300 mm
3D-SOCs (hybrid bonding)	50-500nm@3σ (die corners)	ISO-3 (ISO-2)	1-5 kCPH	ϕ 300 mm
Transfer Printing (mass transfer)	0.5-2µ@3σ (die corners)	ISO-5 (ISO-4)	50–300 kCPH	650 x 550 mm (920 x 730 mm)

Table 1: Heterogeneous integration applications driving enhanced capabilities of advanced die attach equipment

The challenging combinations of required capabilities in table 1 are:

1) Wafer level based sub-micron accuracy for a hybrid bonding C2W process starting with 500nm@3σ down to 50nm@3σ in combination with ISO-3 clean capability, driving down to ISO-2 with throughput demand starting at 1000 CPH, driving to 5000 CPH.
2) Low end panel level applications: fan-out pick and place at typical 5µ@3σ accuracy (3-10µ@3σ) with high throughput demand, starting with 15.000 CPH, driving to 40.000 CPH (picked from one wafer)
3) Bridge embedding on 650 x 550mm panels with 2µ@3σ accuracy (driving down to 0.5µ@3σ) with required throughput of 2000 CPH, driving to 5000 CPH.
4) Transfer printing of micro devices on GEN-3 panels (650 x 550mm) with 2µ@3σ accuracy, driving down to 0.5µ@3σ on GEN-4.5 panels (920 x 730 mm) and beyond with required throughput of 50.000 CPH driving to 300.000 CPH.

Such challenging requirements are asking for disruptive approaches in Advanced Die Attach equipment development.

7. Advanced Gantry System

Advanced Die Attach equipment based on dual gantry system has been successfully deployed for flip-chip, fan-out and thermo-compression applications. Especially for panel level pick and place the gantry approach is easy to scale, although there are challenges that the dominant eigen frequency of a gantry beam scales roughly down with the 2nd power of the beam length, which needs some design measures to keep the eigen frequencies of the beam beyond the band width of the servo control loop.

To support enhanced accuracy on sub-micron level at GEN-3 panel area (650 x 550mm) a disruptive approach for the metrology of an advanced gantry system has been chosen. In

contrast to the classical approach used by many equipment manufacturers, concluding the position of the tool center point from encoder readings which measure the position of several carriages of the gantry, a de-coupled metrology is provided, which is able to measure the tool center point on a more direct way, excluding deformations of the gantry structures caused by heat injection from the motor drives. In addition the gantry system is equipped with water cooling in order to prevent heat flow from the motor drives into the gantry structures, and from there over convection to the metrology beams. Such principle can work very effectively for cold bonding processes, like mass reflow flip chip pick and place, some fan-out pick and place (like eWLB) and hybrid bonding. But even for fan-out or bridge embedding processes requiring constant bond heat (top-heat) the approach with a decoupled metrology is effective.

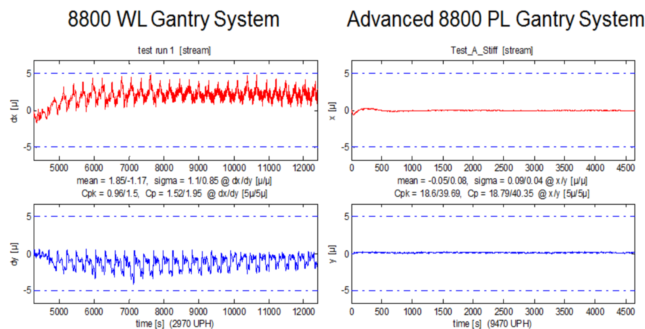

Figure 8: Comparison of x/y-drift at tool center point between conventional 8800 wafer level gantry system (left, 3-4µm drift) and advanced panel level gantry system (right, 0.5µm drift).

The impact on improvement for an advanced gantry system compared to a state-of-the-art gantry system can be seen in figure 8, where coordinate system scaling error drifts in the range of 3-4 µm are reduced to about 0.5µm using the combination of separate metrology beams and water cooling of the motors. It should be noted that the graphs of figure 8 refer to the capability to move to reference positions in the machine with a moving camera, and not to the final placement accuracy. The system of figure 8 is in prototype stage with an initial target to reach 2µ@3σ global placement accuracy on a GEN-3 panel area of 650 x 550 mm, and 1µ@3σ global placement accuracy in a roadmap development.

8. Nanoscale Placement Accuracy

If global placement accuracy (pick and place process which cannot align on local fiducial marks) is not required and local placement accuracy is sufficient, a method called "Van Gogh Alignment" can be applied, which uses a direct metrology to measure die misalignment before placing. An idea of the "Van Gogh Alignment" method is given in figure 9 and described in detail in [29].

The core idea of this method is based on glass based tool reference marks which can both be seen with an upward camera and a downward camera. As shown in figure 9 this enables the upward camera to measure the position of some die fiducial relative to the tool reference mark in the same calibrated feld-of-view (FOV).

The bond head is mounted on a nano-scale x/y-actuator ("Nano Actuator"), which is mounted on a large scale x/y/z gantry system that can move over large areas like 300mm wafer or GEN-3 panel areas. When the position of a substrate fiducial is determined, the Nano Actuator moves the bond head to a standby position to enable the optical path from the substrate fiducial to the downward camera FOV.

After capturing the substrate fiducial position the Nano Actuator moves the bond head close to the target position, which enables the downward camera (which did not move) to capture the tool reference mark additionally, thus allowing to measure the final distance of substrate fiducial und tool reference mark in the same calibrated FOV.

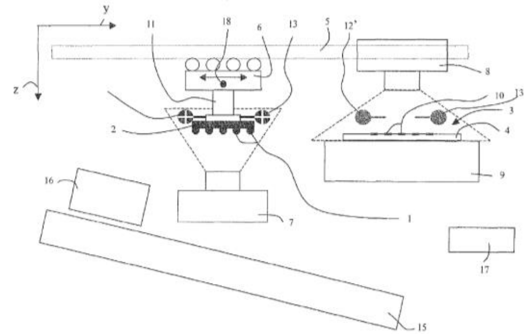

Figure 9: "Van Gogh Alignment": a) upward camera determines the position of die fiducial relative to tool reference mark; b) downward camera determines position of tool reference mark relative to substrate fiducial.

It is worth to realize the following details

1) Since the metrology of distance measurement of two marks in the same calibrated field of view is very accurate, the "Van Gogh Alignment" method is a very accurate approach to determine a final die-to-substrate misalignment.
2) Measurement of die-to-substrate misalignment can even be applied if the z-distance of die to substrate is very small, like 10-50µm
3) After x/y-correction with the Nano Actuator and theta correction, the measurement of final die-to-substrate misalignment can be repeated as a kind of pre-bond inspection, eventually can the whole procedure be iterated before final placement, to guarantee utmost yield.
4) Further the strokes of the Nano Actuator can be designed to be relatively small, which is an optimal condition for achieving nano-scale placement accuracy.
5) If the "Van Gogh Alignment" system is combined with an Advanced Gantry System, as described in the previous section, nano-scale accuracy can also be achieved on a big working area like for GEN-3 panels (650 x 550 mm).

Feasibility studies with glass materials show that the "Van Gogh Alignment" method is capable to align 29x29mm glass die relative to a glass substrate with 200nm@3σ accuracy (figure 10).

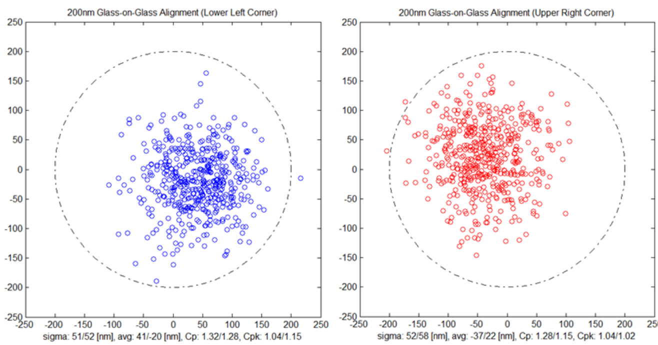

Figure 10: 200nm @ 3σ glass-to-glass alignment process

Verification of such precise alignment can be done by means of an upward camera at the bond location which determines the distance of the two centers of two concentric circles, one belonging to the glass substrate, the other one belonging to the glass die (figure 11).

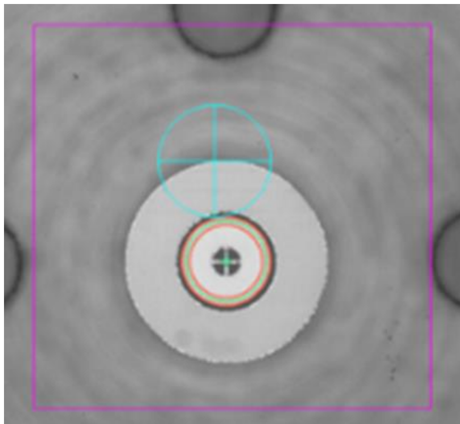

Figure 11: post alignment inspection of glass-to-glass alignment by measuring the center distance of two concentric circles

With a 12 Mega-pixel camera having a FOV of 3.5 x 3.5 mm and a pixel resolution of 0.86 µm the center of a chrome circle on glass with 200 µm diameter can be measured with a repeatability of 30 nm @ 3σ. A ring fiducial on a silicon die with 60µ outer diameter can be recognized using the same camera with about 60 nm @ 3σ. Based on such corner data an error budget can be established for a "Van Gogh Alignment" based Advanced Die Attach machine, where the designed accuracy process allows 75nm @ 3σ for both upward and downward alignment, and requires that the final correction is repeatable with 55nm @ 3σ. Allowing a placement stochastics of 50 nm @ 3σ and residual nonlinearities of 20 nm the placement process is designed to achieve 200 nm @ 4σ (C_{pk} 1.33).

There is believe that "Van Gogh Alignment" based Advanced Die Attach equipment can be introduced with 200nm @ 3σ placement accuracy supporting a throughput of 1000 CPH. The approach is believed to have sufficient potential for throughput increase up to 5000 UPH in a roadmap, as well as to enhance accuracy up to 50nm @ 3σ.

9. Enhanced Clean Capability

It has been mentioned that the majority of experts believe that sub-micron placement accuracy cannot be achieved reasonably in high volume production by utilization of thermo-compression bonding [17,20], and that a (low temperature) hybrid bonding approach, which is based on Van-der-Waals forces, has to be used instead [17,18,19,20,23]. The term 'hybrid bonding' stands for the combination of dielectric bonding and direct (metal-to-metal, e.g. Cu-to-Cu) bonding. Dielectric bonding (as the first step of hybrid bonding) is based on plasma-activated dielectrics which, when brought together at ambient temperature, will result in an instantaneous bonding caused by Van-der-Waals forces. This makes dielectric bonding highly compatible with nano-scale accurate pick and place processes. The direct bonding (second part of hybrid bonding), i.e. the formation of the direct metal-to-metal bond happens in the subsequent annealing process.

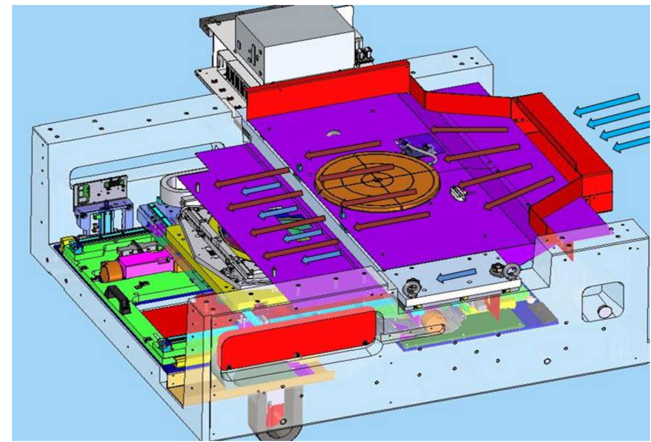

Figure 12: ISO-3 clean-concept for Datacon 8800 platform

Since dielectric bonding takes place at a molecular scale the tolerance for surface contamination is very low. In [20] it is reported that for a C2W hybrid bonding process performed on a Datacon 2200 EVO system the installation of a class 100 (ISO-5) clean kit showed significant yield improvements. For a high volume production solution, however, a clean environment inside of the bonder of class 1 (ISO-3) is being proposed.

Enhancement of clean capability can be achieved by the following measures:

1) Use of ISO-3 compatible cables and vacuum hoses
2) Covering all energy chains and sucking out the dirty air inside of the energy chain covers to an exhaust
3) Introducing a horizontal laminar flow which is cleaned by means of HEPA filters.
4) carrying all materials like substrate wafers or dicing frames in front opening unified pods (FOUPs) and loading them into the equipment via equipment frontend modules (EFEMs) and robots.

Figure 12 shows how the laminar air flow is guided horizontally through a Datacon 8800 Advanced Die Attach machine at two different levels: on the level of the bonding area, and on the level of component picking. The validation of the clean concept for the 8800 platform is still pending, but based on above approaches an implementation of an ISO-3 concept has already

successfully been proven for a Datacon 2200 and an ESEC 2100 platform.

10. Parallel Die Transfer

To enhance throughput beyond 15.000 CPH and to open a perspective for 40.000 CPH, where die picking happens from one single wafer, a concept based on parallel transfer of die has been implemented. An advanced machine concept for a Datacon 8800 platform is based on two gantry systems, each carrying a bond head with multiple nozzles.

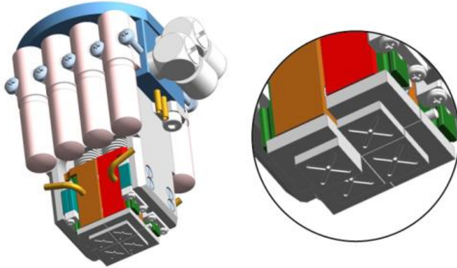

Figure 13: Multi-nozzle bond head concept for 8800 platform

The concept is in the first step implemented for a face-up die attach process with quattro-nozzle heads, where in the standard case 4 dies are picked sequentially from the wafer, are measured in parallel via an upward looking camera, and are bonded sequentially, one after each other. To enable sequential bonding and picking each nozzle can perform an individual 'mini z-stroke' in mm-range, while the whole bond head is mounted on a common theta axis which is carried by a z-axis with bigger z-stroke (100-150 mm range) to cover the height difference between substrate and wafer (figure 13).

The synchronization of ejector z-movement and nozzle-z-movement is done by the common z-axis. The individual 'mini z-strokes' of the nozzles are only used to bring sequentially one of the four nozzles into working or standby position. With such concept a throughput up to 20.000 CPH can be achieved on Gen-3 panel size for 10-15µm @ 3σ with moderate effort.

11. Conclusions

Heterogeneous Integration is in the near future to be considered as a substitute for Moore's law scaling in order to achieve significant cost and power reduction per electronic function. Since Advanced Die Attach will in future be a key process for Heterogeneous Integration, disruptive developments are necessary to achieve placement accuracy in the nano-scale. Front-end like clean capability (ISO-3/ISO-2) is required to enable C2W hybrid bonding. At the same time it is desired to scale up working areas for GEN-3 panels and larger, while boosting throughput beyond 20.000 CPH. Mass transfer of micro devices using transfer printing, requiring placement accuracies close to 1µ @ on large panel sizes, is key to boost throughput beyond 100.000 components per hour.

To drive developments into the required direction four disruptive developments for Advanced Die Attach equipment have been proposed: an Advanced Gantry System based on decoupled metrology and water cooling, which offers global placement accuracy in the 1µ @ 3σ range, the 'Van Gogh Alignment' method, offering a placement accuracy roadmap down to 50nm @ 3σ range, equipment improvements to achieve front-end like clean capability (ISO-3/ISO-2), and a parallel die transfer method, which allows to boost throughput up to the 40.000 CPH range.

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